|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | | Signals | | | | | | | | | |
| RegDst | Jump | branch | branchnot | MemRead | MemtoReg | ALUop | MemWrite | ALUSrc | RegWrite |
| R-Type | add | 01 | 0 | 0 | 0 | 0 | 00 | 10 | 0 | 0 | 1 |
| sub |
| mult |
| and |
| or |
| xor |
| slt |
| mfhi |
| mflo |
| Jr |
|  | lw | 00 | 0 | 0 | 0 | 1 | 01 | 00 | 0 | 1 | 1 |
| sw | xx | 0 | 0 | 0 | 0 | xx | 00 | 1 | 1 | 0 |
| addi | 00 | 0 | 0 | 0 | 0 | 00 | 00 | 0 | 1 | 1 |
| slti | 00 | 0 | 0 | 0 | 0 | 00 | 01 | 0 | 1 | 1 |
| beq | xx | 0 | 1 | 0 | 0 | xx | 01 | 0 | 0 | 0 |
| bne | xx | 0 | 0 | 1 | 0 | xx | 01 | 0 | 0 | 0 |
| J | xx | 1 | x | x | 0 | xx | xx | 0 | x | 0 |
| Jal | 10 | 1 | x | x | 0 | 10 | xx | 0 | x | 1 |

|  |  |  |  |
| --- | --- | --- | --- |
|  | | Inst [31:26] | Inst [5:0] |
| R-Type | add | 000000 | 100000 |
| sub | 000000 | 100010 |
| mult | 000000 | 011000 |
| and | 000000 | 100100 |
| or | 000000 | 100101 |
| xor | 000000 | 100110 |
| slt | 000000 | 101010 |
| mfhi | 000000 | 010000 |
| mflo | 000000 | 010010 |
| Jr | 000000 | 001000 |
|  | lw | 100011 | - |
| sw | 101011 | - |
| addi | 001000 | - |
| slti | 001010 | - |
| beq | 000100 | - |
| bne | 000101 | - |
| J | 000010 | - |
| Jal | 000011 | - |

|  |  |  |  |
| --- | --- | --- | --- |
|  | | | Instruction[31:0] |
|  | 0 | add R1,R0,R0 | 000000\_00000\_00000\_00001\_00000\_100000 |
| 4 | addi R2,R0,10 | 001000\_00000\_00010\_0000000000001010 |
| 8 |  |  |
| 12 | lw R10,R1(1000) | 100011\_00001\_01010\_0000001111101000 |
| 16 | lw R11,R1(2000) | 100011\_00001\_01011\_0000011111010000 |
| 20 | addi R1,R1,1 | 001000\_00001\_00001\_0000000000000001 |
| 24 |  |  |
| 28 | add R12,R10,R11 | 000000\_01010\_01011\_01100\_00000\_100000 |
| 32 |  |  |
| 36 |  |  |
| 40 | sw R12,R1(2999) | 101011\_00001\_01100\_0000101110110111 |
| 44 | bne R1,R2,-12 | 000101\_00001\_00010\_1111111111110100 |
| Q2 | 0 | addi R20,R0,20 | 001000\_00000\_10100\_0000000000010100 |
| 4 | addi R1,R0,1 | 001000\_00000\_00001\_0000000000000001 |
| 8 | add R8,R0,R0 | 000000\_00000\_00000\_01000\_00000\_100000 |
| 12 | lw R9,R0(1000) | 100011\_00000\_01001\_0000001111101000 |
| 16 | lw R3,R1(1000) | 100011\_00001\_00011\_0000001111101000 |
|  |  |  |
|  |  |  |
| 20 | slt R10,R3,R9 | 000000\_00011\_01001\_01010\_00000\_101010 |
|  |  |  |
|  |  |  |
| 24 | beq R10,R0,2 | 000100\_01010\_00000\_0000000000000010 |
| 28 | add R9,R0,R3 | 000000\_00011\_00000\_01001\_00000\_100000 |
| 32 | add R8,R0,R1 | 000000\_00001\_00000\_01000\_00000\_100000 |
| 36 | addi R1,R1,1 | 001000\_00001\_00001\_0000000000000001 |
|  |  |  |
|  |  |  |
| 40 | bne R1,R20,-7 | 000101\_10100\_00001\_1111111111110011 |
| 44 | sw R9,R0(2000) | 101011\_00000\_01001\_0000011111010000 |
| 48 | sw R8,R0(2004) | 101011\_00000\_01000\_0000011111010100 |